Amendments to the Claims

Listing of Claims

This listing of claims will replace all prior versions and listings of claims in the application:

Claims 1-8 (Cancelled).

9. (Previously presented) A method for fabricating a semiconductor component having a stress-absorbing semiconductor layer, comprising the steps of:

a) forming a carrier material;

b) forming a crystalline stress generator layer having substantially a first lattice constant on the carrier material in order to generate a mechanical stress;

c) forming an insulating stress transmission layer on the stress generator layer for transmitting the mechanical stress that has been generated;

d) forming a crystalline, stress-absorbing semiconductor layer having a second lattice constant, which is different than the first lattice constant, on the stress transmission layer for the purpose of absorbing the mechanical stress;

e) forming a gate dielectric on the stress-absorbing semiconductor layer;

f) forming a control layer on the gate dielectric;

g) patterning the gate dielectric and the control layer; and

h) forming source/drain regions in the stress-absorbing semiconductor layer.

10. (Previously presented) The method as recited in claim 9, wherein in step a) the semiconductor substrate having a (100) surface orientation is provided, and a semiconductor buffer layer is epitaxially deposited thereon in order to produce a smooth surface.

11. (Previously presented) The method as recited in claim 9, wherein in step b) a IV-IV or III-V semiconductor is used.

12. (Previously presented) The method as recited in claim 11, wherein in step b) a multiple layer sequence is formed as the stress generator layer.

13. (Previously presented) The method as recited in claim 9, wherein in step b) the stress generator layer is smoothed by means of a molecular beam epitaxy process.

14. (Previously presented) The method as recited in claim 9, wherein in step c) a crystalline insulator layer is formed as the stress transmission layer.

15. (Previously presented) The method as recited in claim 14, wherein in step c) the stress transmission layer with a lattice constant which is matched to the second lattice constant of the stress-absorbing semiconductor layer is formed.

16. (Previously presented) The method as recited in claim 15, wherein in step c) only a few atom layers of the stress transmission layer are deposited epitaxially on the stress generator layer.

17. (Previously presented) The method as recited in claim 9, wherein in step d) a fully depleted semiconductor material is used.

18. (Previously presented) The method as recited in claim 9, wherein in step e) a material with a high dielectric constant is used as the gate dielectric.

19. (Previously presented) The method as recited in claim 9, wherein in step f) a metal is used as the control layer.

20. (Previously presented) The method as recited in claim 9, wherein
in step a) Si is used as the carrier material;
in step b) SiGe is used as the stress generator layer;
in step c) CaF_2 is used as the stress transmission layer;

in step d) Si is used as the stress-absorbing semiconductor layer;

in step e) HfO_2 is used as the gate dielectric; and

in step f) TiN is used as the control layer.